

2304SRG



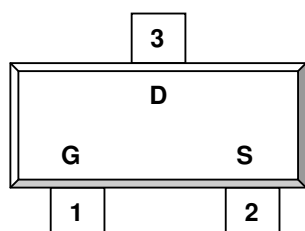
N Channel Enhancement Mode MOSFET

3.2A

DESCRIPTION

2304SRG is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION SOT-23

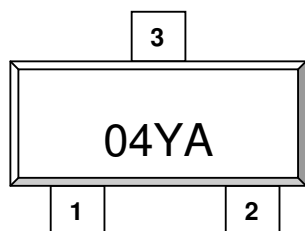


1.Gate 2.Source 3.Drain

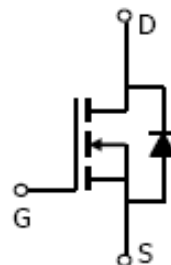
FEATURE

- 30V/3.2A, $R_{DS(ON)} = 44\text{m-ohm}$ (Typ.) @VGS = 10.0V
- 30V/2.0A, $R_{DS(ON)} = 60\text{m-ohm}$ @VGS = 4.5V
- 30V/1.5A, $R_{DS(ON)} = 90\text{ m-ohm}$ @VGS = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PART MARKING SOT-23



Y: Year Code A: Process Code



ORDERING INFORMATION

Part Number	Package	Part Marking
2304SRG	SOT-23	04YA

※ Process Code : A ~ Z ; a ~ z

※ 2304SRG S : SOT-23 ; R : Tape Reel ; G : Pb – Free

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3.2A**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	30	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	3.2 2.6	A
Pulsed Drain Current		I _{DM}	10	A
Continuous Source Current (Diode Conduction)		I _S	1.20	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	1.20 0.8	W
Operation Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	100	°C/W

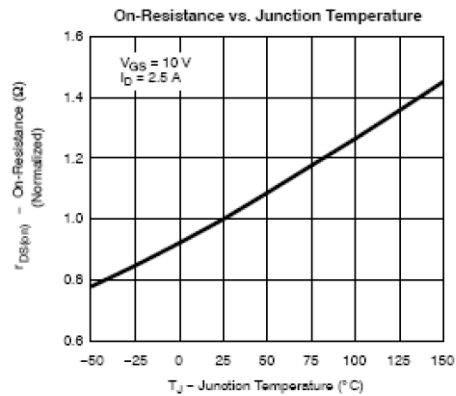
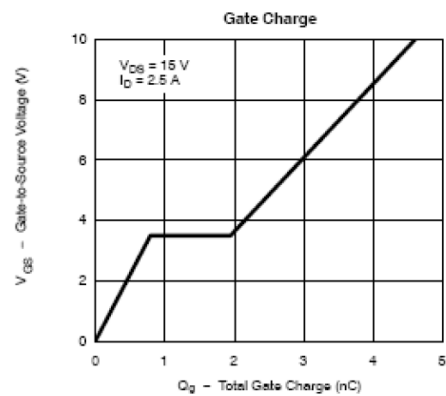
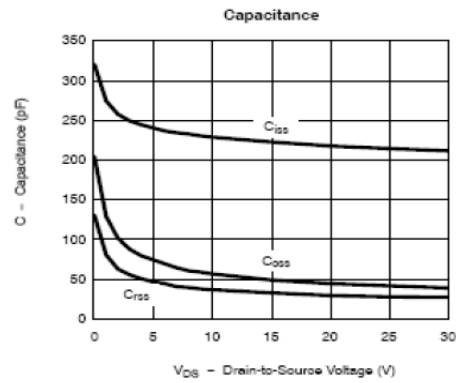
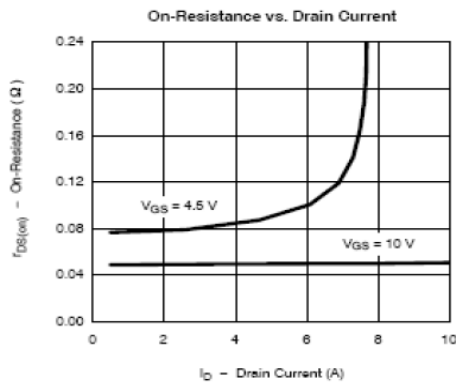
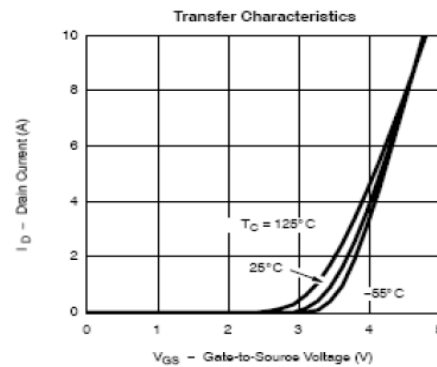
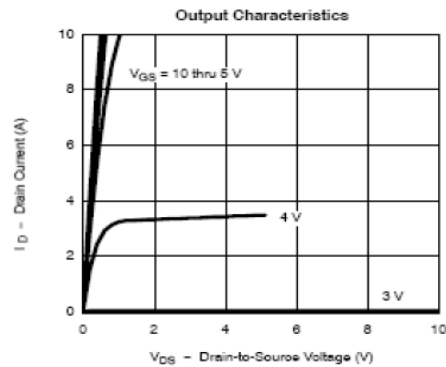
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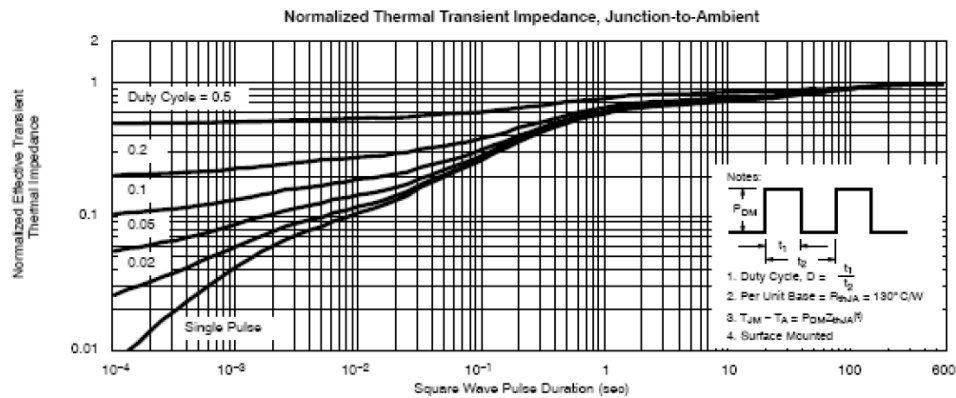
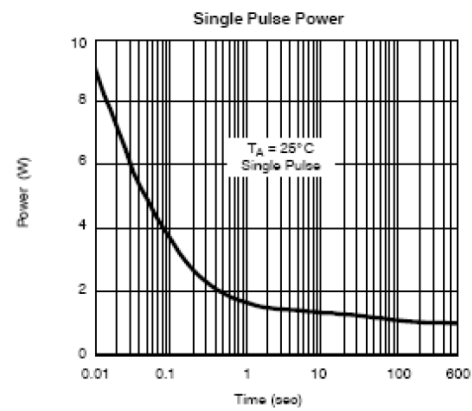
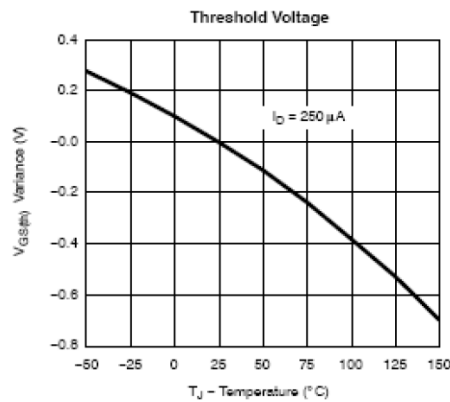
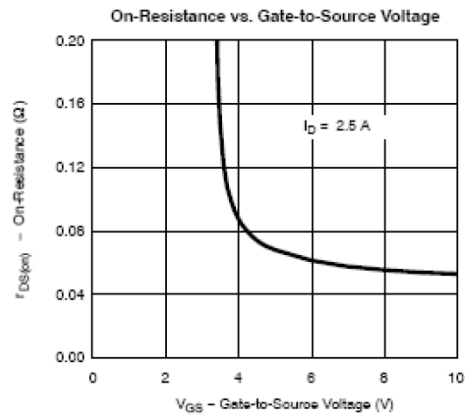
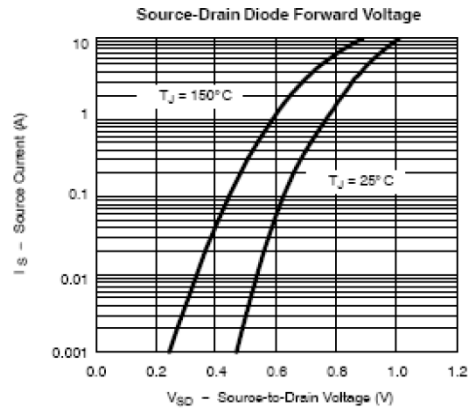
3.2A**ELECTRICAL CHARACTERISTICS** ($T_a = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=1.0V$			1	uA
		$V_{DS}=30V, V_{GS}=0V$ $T_J=55^{\circ}C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 4.5V, V_{GS}=10V$ $V_{DS}\geq 4.5V, V_{GS}=4.5V$	6 4			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.2A$ $V_{GS}=4.5V, I_D=2.0A$ $V_{GS}=2.5V, I_D=1.5A$		0.044 0.060 0.090	0.052 0.067 0.100	Ω
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=2.5V$		4.6		S
Diode Forward Voltage	V_{SD}	$I_S=1.25A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V$ $V_{GS}=10V$ $I_D\equiv 2.5A$		4.5	10	nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=15V$ $V_{GS}=0V$ $F=1MHz$		240		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			17		
Turn-On Time	$t_{d(on)}^{tr}$	$V_{DD}=15V$ $R_L=15\Omega$ $I_D=1.0A$ $V_{GEN}=10V$ $R_G=6\Omega$		8.0	20	nS
				12	30	
Turn-Off Time	$t_{d(off)}^{tf}$			17	35	
				8.0	20	

TYPICAL CHARACTERISTICS (25°C Unless noted)

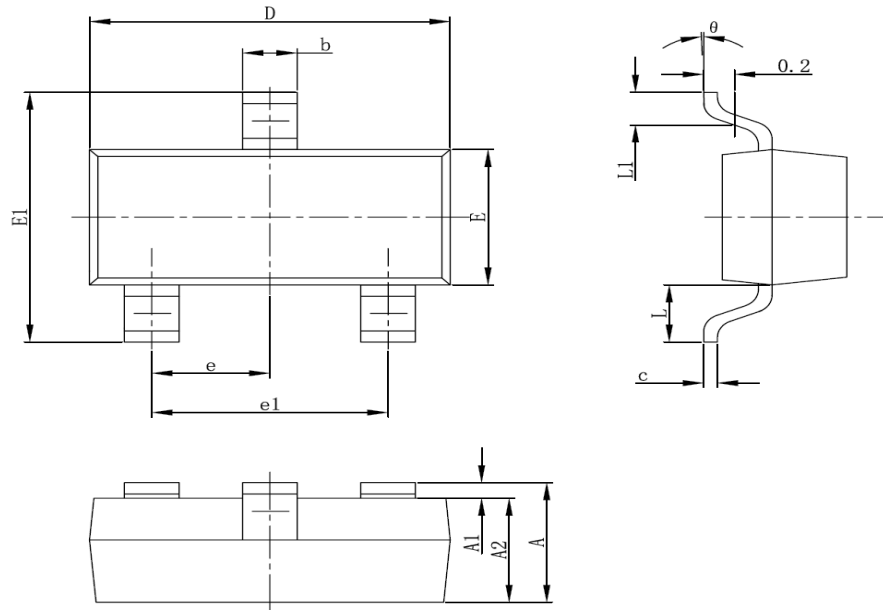


TYPICAL CHARACTERISTICS (25°C Unless noted)



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3.2A**SOT-23 PACKAGE OUTLINE**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°