3402

Lead-free

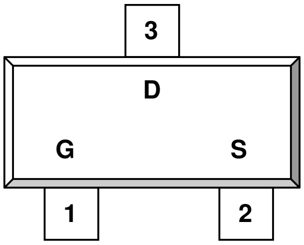
N Channel Enhancement Mode MOSFET

4.0A

DESCRIPTION

3402 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION
SOT-23-3L

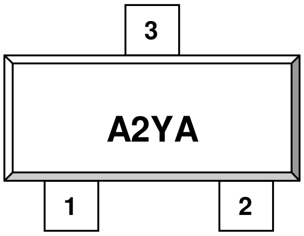


1.Gate 2.Source 3.Drain

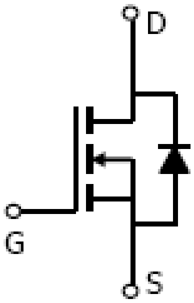
FEATURE

- 30V/2.8A, $R_{DS(ON)}$ = 48mΩ @V_{GS} = 10V
- 30V/2.3A, $R_{DS(ON)}$ = 53mΩ @V_{GS} = 4.5V
- 30V/1.5A, $R_{DS(ON)}$ = 80mΩ @V_{GS} = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

PART MARKING
SOT-23-3L



Y: Year Code A: Week Code



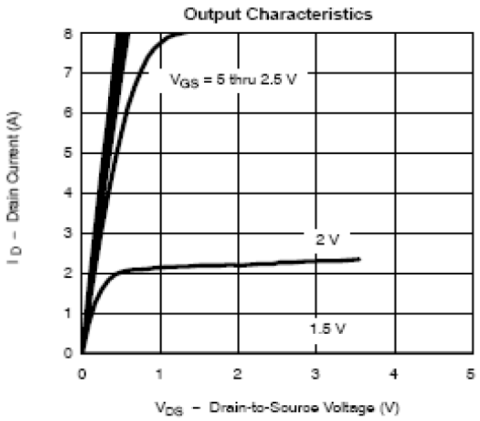
ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

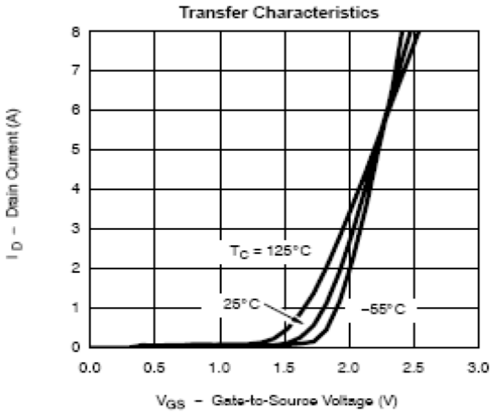
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain CurrentTJ=150℃)	T_A=25℃ T_A=70℃	I_D	4.0 2.8	A
Pulsed Drain Current		I_{DM}	10	A
Continuous Source Current (Diode Conduction)		I_S	1.25	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

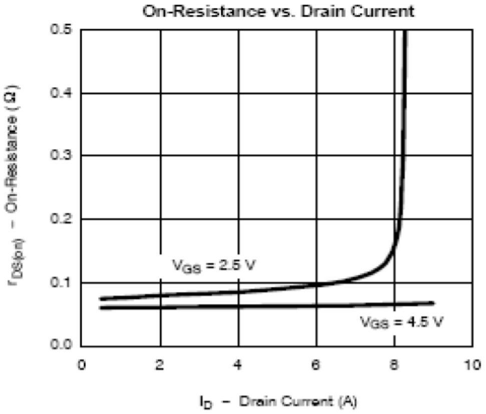
ELECTRICAL CHARACTERISTICS (Ta = 25℃ unless otherwise noted)

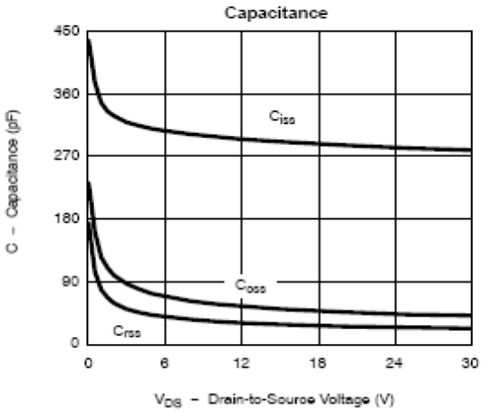
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=250uA	0.8		1.6	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V			1	uA
		V_{DS}=24V,V_{GS}=0V T_J=55℃			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geqq$4.5V,V_{GS}=4.5V	4			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2.8A V_{GS}=4.5V,I_D=4.5A V_{GS}=2.5V,I_D=1.5A		48 53 80		mΩ
Forward Transconductance	g_{fs}	V_{DS}=4.5V,I_D=5.8A		12		S
Diode Forward Voltage	V_{SD}	I_S=1.25A,V_{GS}=0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=15V V_{GS}=4.5V $I_D \equiv$2.0A		4.2	6	nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	V_{DS}=15V V_{GS}=0V F=1MHz		350		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			41		
Turn-On Time	$t_{d(on)}$	V_{DD}=15V R_L=10Ω I_D=1.0A V_{GEN}=10V R_G=3Ω		2.5		nS
	t_r			2.5		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			4		

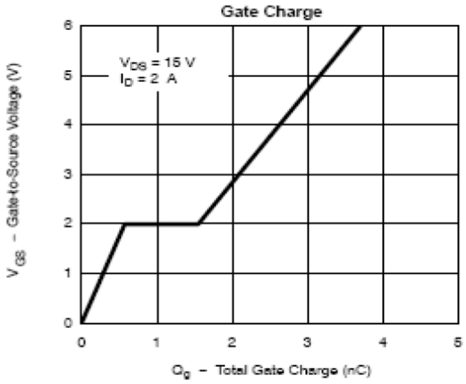
TYPICAL CHARACTERICTICS (25℃ unless otherwise noted)

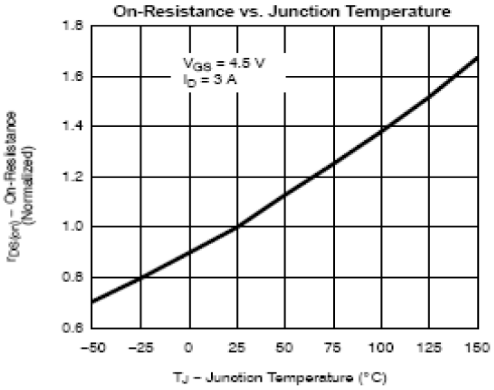

Output Characteristics


Transfer Characteristics

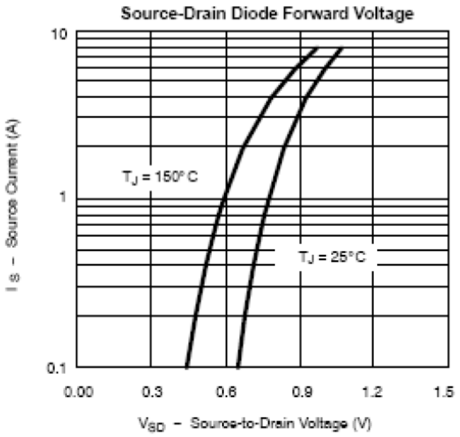

On-Resistance vs. Drain Current

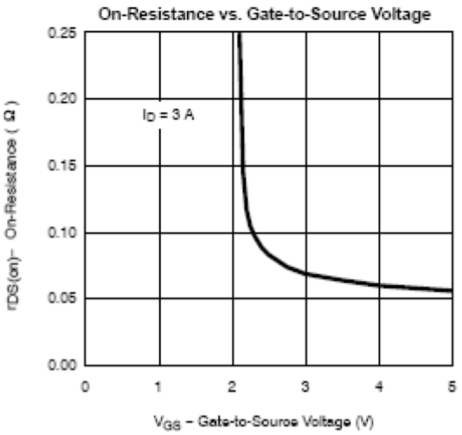

Capacitance

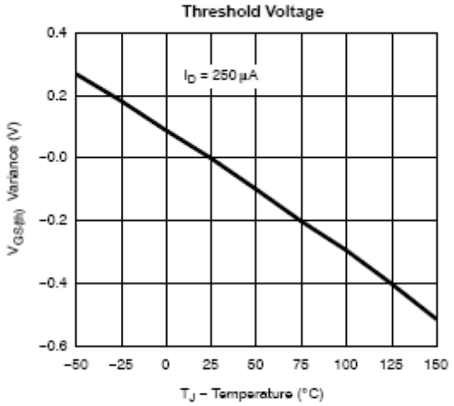

Gate Charge

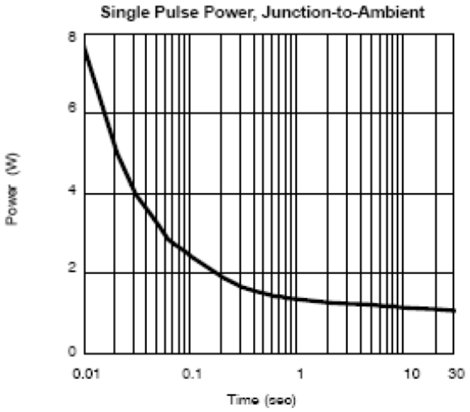

On-Resistance vs. Junction Temperature

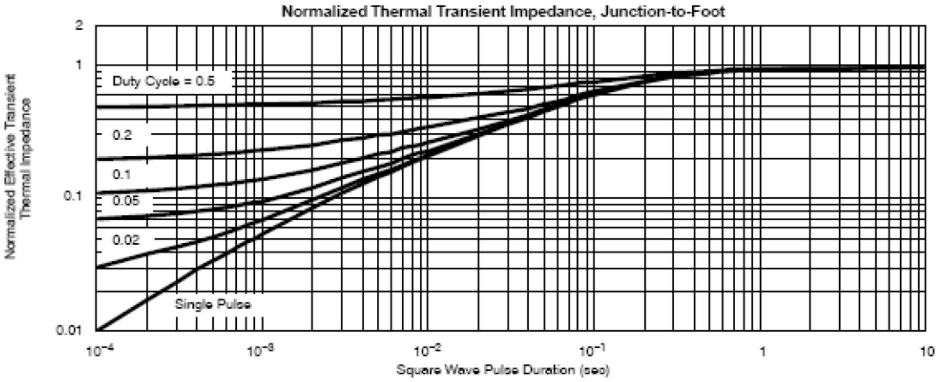
TYPICAL CHARACTERICTICS (25℃ unless otherwise noted**)**


Source-Drain Diode Forward Voltage

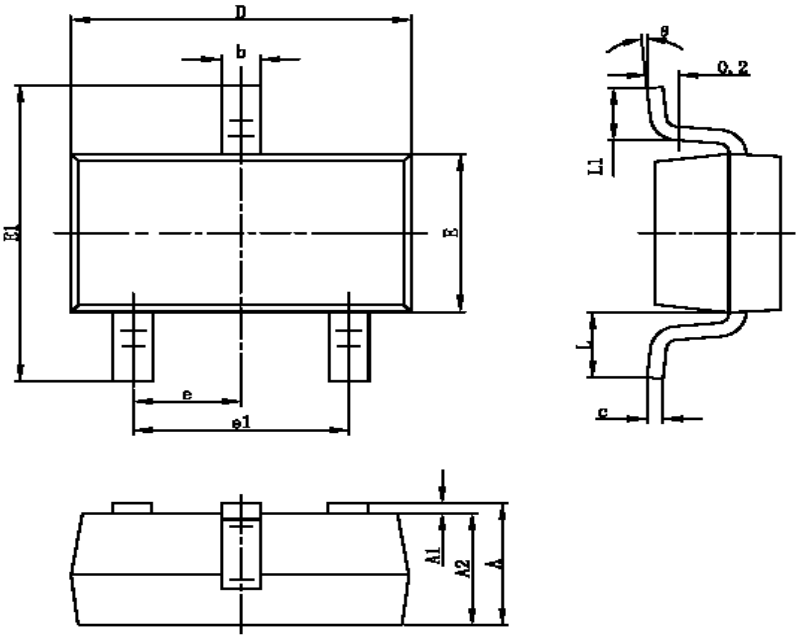

On-Resistance vs. Gate-to-Source Voltage


Threshold Voltage


Single Pulse Power, Junction-to-Ambient


Normalized Thermal Transient Impedance, Junction-to-Foot

SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°